Progress and Outlook for MRAM Technology

S. Tehrani, J.M. Slaughter, E. Chen, M. Durlam, J. Shi, and M. DeHerrera
Motorola Labs, Physical Sciences Research Laboratories

Abstract—We summarize the features of existing semiconductor memories and compare them to Magnetoresistive Random Access Memory (MRAM), a semiconductor memory with magnetic bits for nonvolatile storage. MRAM architectures based on Giant Magnetoresistance (GMR) and Magnetic Tunnel Junction (MTJ) cells are described. This paper will discuss our progress on improving the material structures, memory bits, thermal stability of the bits, and competitive architectures for GMR and MTJ based MRAM memories as well as the potential of these memories in the commercial memory market.

Index terms— Giant magnetoresistance, GMR, magnetic tunnel junction, MTJ, magnetoresistive random access memory, MRAM

I. INTRODUCTION

THERE are many types of memories in the VLSI arena. Table 1 shows a comparison of MRAM expected features with other semiconductor memory technologies. Figure 1 shows the general architecture of each of these technologies. Each has important advantages as well as shortcomings. For example, SRAM has very fast read and write speeds, but it is volatile and requires a minimum of four transistors per cell. Therefore, current state-of-the-art SRAM requires a relatively large cell area of approximately $40F^2$, where F is minimum feature geometry. DRAM cell architecture is simpler and denser than SRAM, requiring one pass transistor and a storage capacitor per cell. DRAM has moderate read/write speeds and the cell size is currently about $10F^2$. The charge in the capacitor leaks through the pass transistor and needs to be refreshed in millisecond time intervals. Flash is a high-density ($8F^2$) nonvolatile memory technology in which the charge is stored in a dummy gate. Flash NAND architecture is shown in Figure 1. In read mode, Flash has unlimited endurance, operates at low voltages, and has moderate access times. However, in write mode, Flash has limited endurance of 10^5-10^6 cycles, requires high voltage (5-12 V), and has slow program (ms) and erase (sec) times. Flash die efficiency, the ratio of memory core to peripheral support circuitry, does not compete with DRAM because of the high voltage circuit requirements.

Magnetoresistive Random Access Memory (MRAM) is based on the integration of Si CMOS with magnetic memory elements. MRAM is nonvolatile and has unlimited read and write endurance. Recent advances in Giant Magnetoresistance (GMR) [1] - [4] and Magnetic Tunnel Junction (MTJ) [5] - [7] materials give MRAM the potential for high speed, low operating voltage, and high density.

This paper describes our progress on the material structures, thermal stability, switching characteristics, and competitive architectures for GMR and MTJ based MRAM memories as well as the potential of these memories in the commercial memory market.

Table 1. Comparison of MRAM expected features with other memory technologies.

	SRAM	*DRAM*	*FLASH*	*MRAM*
Read Time	fast	mod.	mod.	mod.-fast
Write Time	fast	mod.	slow	mod.-fast
Non-Volatile	no	no	yes	yes
Refresh	NA	ms	NA	NA
Minimum Cell Size	large	small	small	small
Low Voltage	yes	limited	no	yes

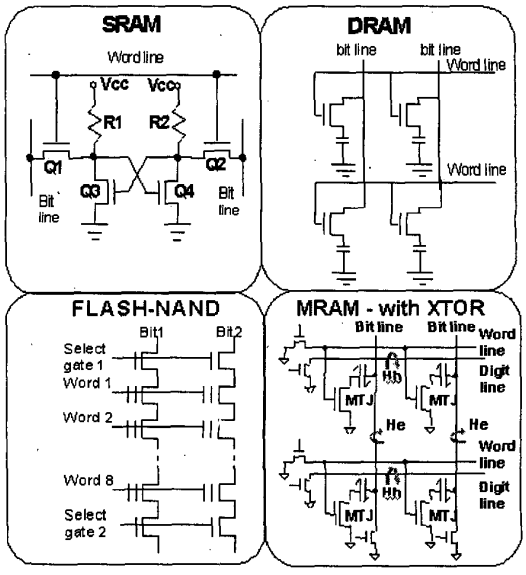

Figure 1. Cell architecture schematics for semiconductor memory technologies.

II. MRAM MEMORY ARCHITECTURES

We have studied various submicron GMR and MTJ memory elements and their possible memory cell architectures. The two kinds of Current-In-Plane (CIP) GMR structures we considered are the spin valve and the pseudo

Manuscript received March 21, 1999.
2100 East Elliot Road, Tempe, AZ 85284
This work was supported in part by DARPA.

spin valve (PSV). Memory architecture using GMR spin valve, Figure 2, requires a single pass transistor per cell [8], [9] for non-destructive read. In the spin valve memory element one of the magnetic layers is pinned while the other layer is free to change polarization, this free layer stores the information based on the direction of magnetic polarization with respect to the pinned layer. In this architecture, the resistance of the GMR storage element is compared with a reference cell to determine the state of the memory. The GMR sheet resistance is low (~15 Ω/sq) and large currents (>1 mA) are required from the pass transistor in order to achieve reasonable signal levels. The current that is required from the pass transistor is larger than the current achieved by a minimum geometry transistor. Therefore, the large pass transistor dominates the cell area and the resulting cell size is not competitive with high-density memory technologies.

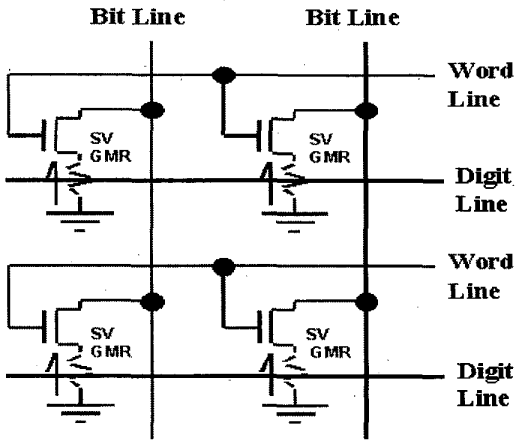

Figure 2. GMR based MRAM architecture using a spin valve with one transistor per memory bit.

The PSV structure consists of two magnetic layers of different thickness with Cu as an interlayer. The different thickness magnetic layers have different switching fields due to the shape anisotropy at submicron dimensions [10]. The magnetic moments of the two magnetic layers can be predominantly anti-parallel or parallel, making the resistance of the film high or low respectively. A typical PSV structure and its electrical characteristic are shown in Figure 3. The magnetoresistance ratio of these sandwich films ranges from 6% to 9%.

A PSV memory cell stores information in the two possible polarization states of the thick magnetic layer (Figure 3). The bit is read non-destructively by applying a sense current together with a negative and then a positive digit current. The digit current magnitude is chosen such that the magnetic field generated by the digit current and the sense current combined is enough to switch the thin magnetic layer, but not enough to switch the thick magnetic layer.

In the GMR-PSV memory architecture, a number of GMR memory elements can be stacked in series with a single pass transistor, as shown in Figure 4. This is the most viable GMR architecture, because it provides an opportunity for a high-density memory that is not limited by the area of the pass transistor. For read the operation, the amplifier is first auto-zeroed, then the sense current is applied to the stack of active and reference bits while a negative digit current is applied to the active memory bit. The sense currents remain on while the digit current is switched to the positive direction and the output of the amplifier is strobed. The bit information is determined by detecting the change in signal magnitude between the active bit cell and the reference cell [11].

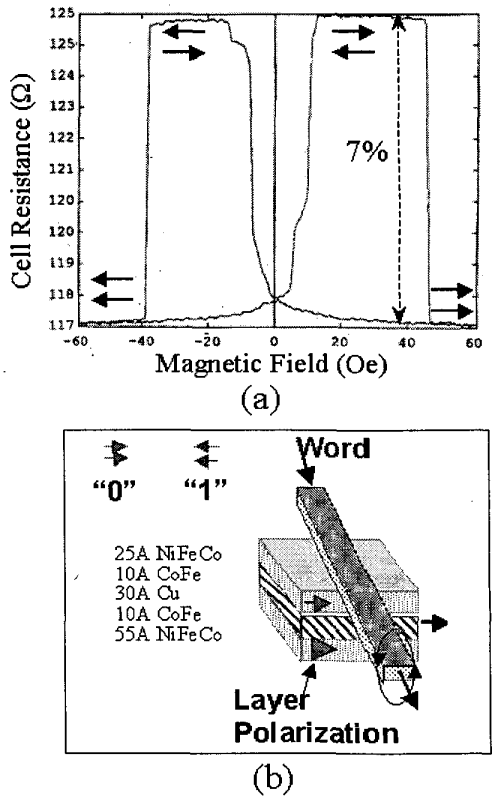

Figure 3. GMR based material structure, (a) shows a typical R-H characteristic for a 0.6x3.6μm^2 cell; (b) shows a typical GMR material stack.

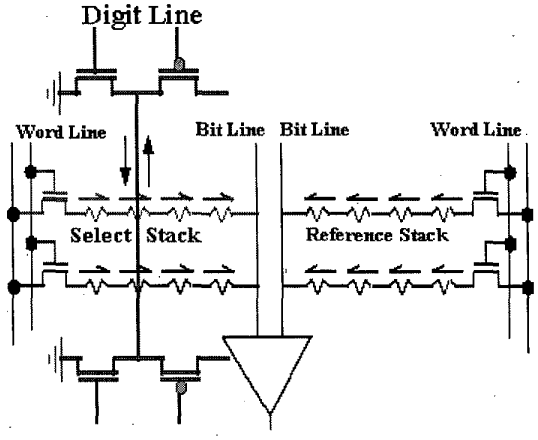

Figure 4. GMR based MRAM architecture using a Pseudo-Spin Valve requires only one transistor per memory bit stack.

A typical Current-Perpendicular-to-Plane (CPP) MTJ structure is shown in Figure 5. In the case of MTJ-based MRAM, the resistance of the cell is large and the sense currents are small (μA range). It is therefore viable to use a minimum sized active device (transistor or diode [18]) as the isolation device in conjunction with a MTJ spin valve element to define the MRAM cell (Figure 1). The cell area in this architecture can be defined by the larger of the active device or the MTJ cell. The MTJ spin valve uses the direction of polarization of the free layer for information storage. The resistance of the memory bit is either low or high dependent on the relative polarization, parallel or anti-parallel, of the free layer with respect to the pinned layer (Figure 5). Uniformity of the MR ratio and the absolute resistance of the cell are critical in this architecture, since the absolute value of the MTJ resistance is compared with a reference cell during read mode. If the active device resistances in a block of a memory show a large resistance variation, a signal error can occur when they are compared with a reference cell. The resistance of the MTJ cell is exponentially dependent on the thickness of the AlOx barrier. Therefore it is anticipated that small variations in the AlOx thickness would result in large variations in the resistance.

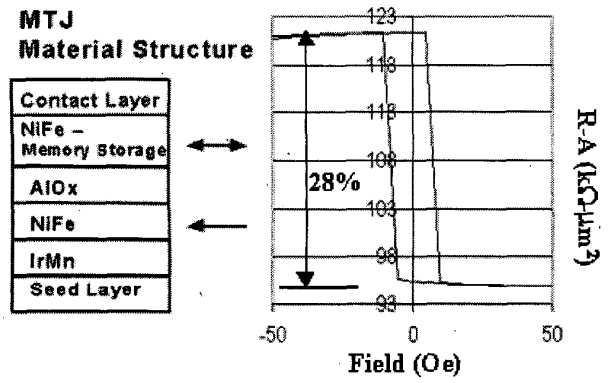

Figure 5. Typical MTJ material stack and R-H characteristic for a memory bit.

Figure 6 shows the results from an experiment on array uniformity across a six inch wafer. Shown in the figure are (6a) the schematic of the array consisting of 18 10x10μm^2 bits and covering an area of 1mmx1.2mm; (6b) the median resistance of the bits; (6c) the absolute variation from maximum to minimum for parallel state resistance of the bits; (6d) and the usable MR within each array. Usable MR is the MR available for use by the circuit as defined in equation 1, where $R_{\uparrow\downarrow Min}$ is the minimum measured anti-parallel state resistance in the array, and $R_{\uparrow\uparrow Max}$ is the maximum measured parallel resistance state in the array. This material had an original MR of about 34%. This data shows that even though the cell resistance varies by a factor of about 1.8 across the wafer, we are still able to get enough uniformity within each array to obtain greater than 27% usable MR.

$$MR_{usable} = \frac{R_{\uparrow\downarrow Min} - R_{\uparrow\uparrow Max}}{R_{\uparrow\uparrow Max}} \quad (1)$$

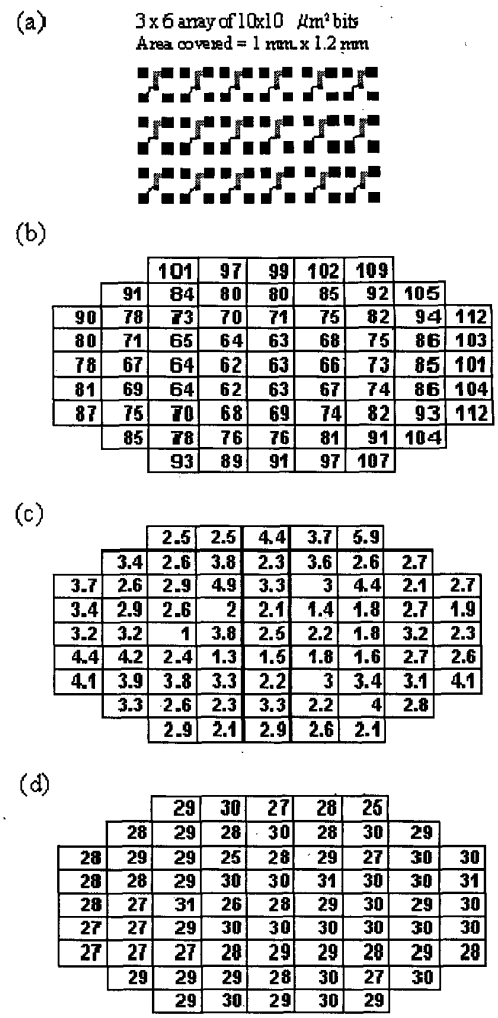

Figure 6. (a) Schematic of the uniformity array. (b) Median resistance of bits in each array. (c) Variation in bit parallel state resistances in each array. (d) Usable MR within each array.

III. MRAM MATERIAL CHARACTERISTICS

A. *Thermal Characteristics*

One of the challenges involved in the integration of MRAM technology is the temperature compatibility with CMOS processes. This means that either the magnetic materials must be made to withstand standard backend process temperatures, or low-temperature processes must be developed for MRAM technology.

Figure 7 shows the response of PSV-GMR bits to bake temperature. Each data point represents the average of about

100 bits across two wafers. The two wafers were exposed consecutively to each temperature for 5 minutes. We observe good stability to 300 °C followed by a sharp drop in signal of more than 30% by 400 °C. These results are comparable to the best thermal stability results published on similar spin valve structures.[12], [13]. The change in resistance is actually constant between each temperature, so it is likely that much of the signal loss is due to increasing bit resistance caused by the intermixing of the magnetic layers with the Cu spacer layer.

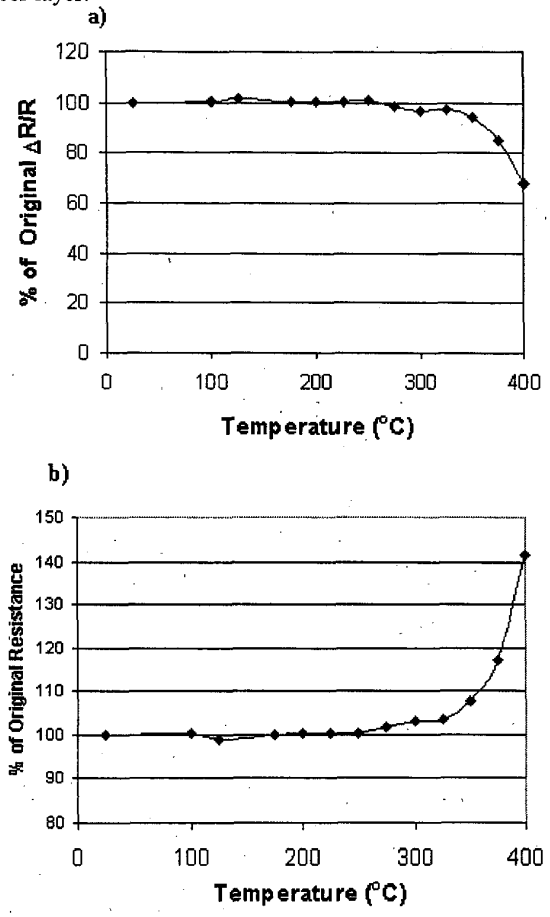

Figure 7. Temperature response of PSV-GMR bits: (a) change in MR vs. Temperature and (b) change in Resistance vs. Temperature. Each data point represents the average of about 100 bits across two wafers. The two wafers were exposed consecutively to each temperature for 5 minutes.

Previous studies of MTJ material have shown that the MR initially increases on annealing but begins to decrease at anneal temperatures between approximately 240°C [14]. and 300°C [15]. Figure 8 shows the response of our MTJ bits to anneal temperature. The junction resistance decreases steadily until 330°C and then begins to increase (Figure 8a). The behavior of MR, shown in Figure 8b, exhibits a slow increase, peaking at 275°C, followed by a sharp drop after 300°C. The MR falls to ½ its original value by 330°C and reaches zero at 390°C. Figure 9 shows the switching characteristics of one of the bits from Figure 8 for each of the bakes between 200°C and 350°C. It can be seen that the coercivity and coupling characteristics are relatively unaffected while the signal degrades.

The difference between as-deposited and low-temperature (T<300°C) annealed material is even more dramatic. Figure 10 illustrates the change in the MR transfer curve due to annealing. In this typical case, the MR doubles and the resistance-area product (RA) decreases slightly after a 250°C anneal.

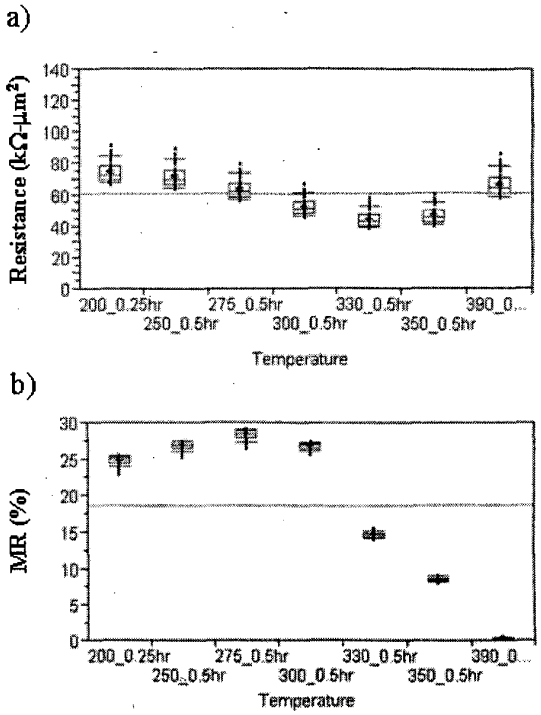

Figure 8. Thermal response of MTJ bits: (a) Resistance vs. Temperature and (b) MR vs. Temperature. Sixty-nine 4x6μm² bits were measured across the wafer after consecutive 30 minute bakes.

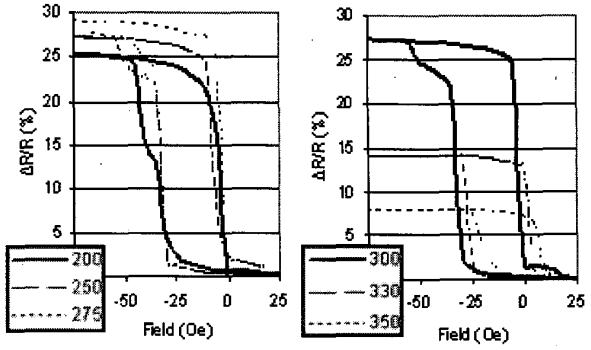

Figure 9. Normalized signal vs. External field curves for 1 4x6μm² bit after various anneal temperatures.

To better understand the changes that occur near the interfaces in the tunnel junction during the initial low-temperature anneal, x-ray photoelectron spectroscopy (XPS) experiments were performed on simplified structures.

Samples consisting of typical bottom electrode layers covered by AlOx were inserted into a UHV chamber for annealing and XPS analysis using a Mg-anode x-ray source and a double-pass cylindrical mirror electron energy analyzer. Figure 11 shows the changes that occur in the photoelectron peaks corresponding to the Fe 2p1/2 and 2p3/2 levels when one sample was annealed at 250°C and 300°C. The large shoulder on the right side of the 2p1/2 peak is due to the presence of oxidized Fe in the vicinity of the AlOx barrier. The chemical state of the iron oxide is unknown, but the peak shift is similar to FeO, rather than Fe_2O_3. On annealing at 250 °C, the FeOx signal is lower, and after the 300°C anneal it is lower still. The raw data had the background removed and was normalized before being fit to separate Fe and FeOx peaks as shown in the figure.

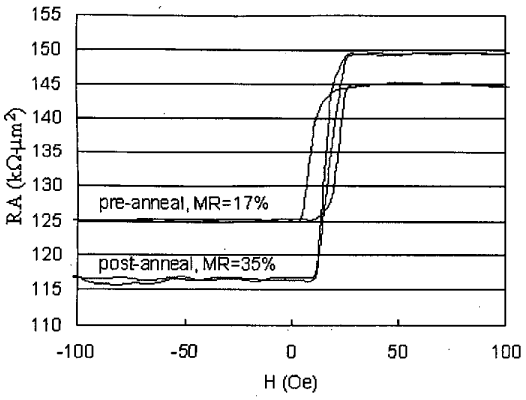

Figure 10. Resistance vs. applied field curves for MTJ material as-deposited and after a 30 min. anneal at 250 °C.

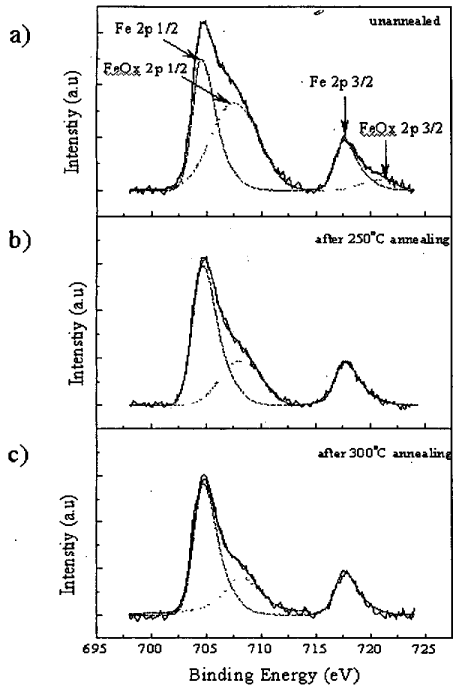

Figure 11. XPS spectra for Si: SiO2 2000/ Ta 50/ NiFe 200/ Al 14.8 (ox) . The contribution from oxidized Fe decreases from a) the as-deposited state, with increasing annealing temperatures, b) 250°C, and c) 300°C.

These results imply that some of the Fe is oxidized together with the Al layer, but is at least partially reduced again to metallic Fe when annealed. The initial state may be due to intermixing of Fe and Al when the Al is deposited. The intermixed Fe is then oxidized together with the Al, giving rise to the large FeOx peak. Since the enthalpy of formation of aluminum oxide is larger (more negative) than iron oxide, the reduction effect could be due to a competition between the Fe and the Al for the available oxygen, which favors the Al.

B. Switching Characteristics

On the submicron scale, magnetization reversal in MRAM structures does not strictly follow the Stoner-Wohlfarth model, which assumes coherent rotation of the magnetization. Switching fields in real structures are often lower than the Stoner-Wohlfarth calculations. Non-uniform magnetization at both ends and at trapped vortices [16], [17] provides additional torque to facilitate the reversal process, therefore, the switching field is lowered.

In the GMR-PSV type of memory, magnetization orientations of both the soft and hard layers need to be reversed for read and write operations, respectively. But in the MTJ approach, only the free layer magnetization needs to be reversed for a write operation, and the other layer is magnetically pinned.

The MRAM cells used in a memory array need to be selectable by the electronics. The pass, or isolation, transistors provide bit selection for reading individual bits. By turning the transistor on or off the bit is selected or deselected for reading. Writing information to the MRAM cells is quite different from reading them. The cell is written by a magnetic field, which is generated by current flowing through a conductor. These conductors are densely packed in the core of a memory and each conductor covers many different bits. The conductors are arranged in a cross point architecture that provides field for switching the bit [18]. The intersection of these cross points generates a peak field, which is sufficient to switch the desired bit. One line provides the field that affects the easy axis of the bit, while another line provides the field that affects the hard axis of the bit. The combination of fields from both lines will create a peak field that is engineered to be just over the switching threshold for the bit.

In PSV structures, sense lines generate hard axis fields, which act in opposite directions on soft and hard layers. As shown in Figure 12, a 1mA sense current causes about 5 Oe reduction in easy axis switching field of the hard layer. In order to achieve full selectivity in an array, the reduction in the easy axis switching field produced by the hard axis field has to be larger than the switching field variation. This can be done either by applying a large enough sense current, or by adding another line that creates an additional hard axis field.

In MTJ structures, the sense current is small and flows perpendicular to the film plane. It cannot be used for select. Bit selectivity can be accomplished by two sets of orthogonal current lines. The characterization of the effects of hard and

easy axis fields are shown in the asteroid curves of Figure 13 for a 0.9μmx1.8μm MTJ device.

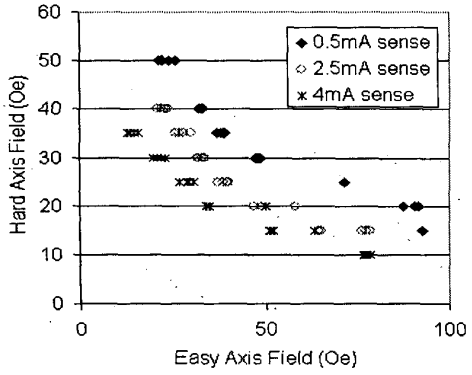

Figure 12. Dual axis switching response of a GMR bit with different sense currents flowing through the bit.

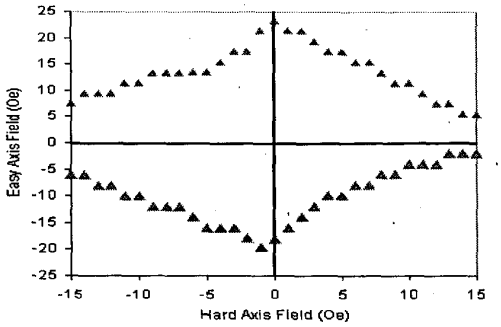

Figure 13. Asteroid curve showing the switching response of a 0.9x1.8μm^2 MTJ bit.

IV. Conclusions

The two most viable MRAM technologies are the PSV and the MTJ approaches. MTJ cells provide a larger signal and have a lower write current than PSV because of the thicker storage layer thickness in the PSV. The advantages of PSV cells are the potential for higher density and apparent advantages in manufacturability. For either approach, significant challenges remain in the areas of magnetic switching, integration with CMOS, and signal uniformity.

Comparison of MRAM with other memory technologies shows that it can be competitive in overall performance. When compared with DRAM it is expected to be favorable due to its non-volatile capability. Overall system power will be reduced since there is no background refreshing required. It is also expected to be comparable in density and read-write performance.

Comparison with SRAM shows that MRAM will be able to compete favorably in cost because of smaller cell size. It also has the non-volatile capability, which is only available in expensive battery backup solutions for SRAM.

When compared with Flash, MRAM achieves much better performance in write characteristics since no high-voltage tunneling mode is required. MRAM endurance also is expected to be better, with no known or expected deterioration mechanism. In addition, there is concern about scaling the size of Flash cells as CMOS geometries decrease[19].

Acknowledgment

The authors acknowledge Charles Falco and David Keavney at the University of Arizona for XPS measurements.

References

[1] M.N. Babich, J.M. Broto, A. Fert, F. Nguyen Van Dau, F. Petroff, P. Eitenne, G. Creuzet, A. Friederich, and J. Chazelas, "Giant magnetoresistance of (100)Fe/(001)Cr magnetic superlattices" Phys. Rev. Lett., vol. 61, pp. 2472-5, 1988.

[2] S. S. P. Parkin, R. Bhadra, and K.P. Roche,"Oscillatory magnetic exchange coupling through thin copper layers", Phys. Rev. Lett., vol. 66, pp. 2152-5, 1991.

[3] W.F. Egelhoff, Jr., P.J. Chen, C.J. Powell, M.D. Stiles, R.D. McMichael, C.-L. Lin, J.M. Sivertsen, J.H. Judy, K. Takano, A.E. Berkowitz, T.C. Anthony, J.A. Brug, J. "Optimizing the giant magnetoresistance of symmetric and bottom spin valves", Appl. Phys., vol. 79, p. 5277, 1996.

[4] J. M. Slaughter, E. Y. Chen, and S. Tehrani, "Magnetoresistance of ion-beam deposited Co/Cu/Co and NiFe/Co/Cu/Co/NiFe spin valves," J. Appl. Phys., vol. 85, pp. 4451-53, 1999.

[5] T. Miyazaki and N. Tezuka, "Giant magentic tunneling effect in Fe/Al2O3/Fe junction," J. Magn. Magn. Mater., vol. 139, L231, 1995.

[6] J.S. Moodera, L.R. Kinder, T.M. Wong, and R. Meservey, "Large magnetoresistance at room temperature in ferromagnetic thin film tunnel junctions," Phys. Rev, Lett., vol. 74, pp. 3273-6, 1995.

[7] W.J. Gallagher, S.S.P. Parkin, Y. Lu, X.P. Bian, A. Marley, R.A. Altman, S.A. Rishton, K.P. Roche, C. Jahnes, T.M. Shaw, and G. Xiao, "Microstructured magnetic tunnel junctions," J. Appl. Phys., vol. 81, pp. 3741-6, 1997.

[8] D.D. Tang, P.K. Wang, V.SA. Speriosu, S. Le, R.E. Fontana, and S. Rishton, "An IC process compatible nonvolatile magnetic RAM," IEDM Tech. Digest. New York: IEEE, 1995, pp. 997-1000.

[9] E. Y. Chen, S. Tehrani, T. Zhu, M. Durlam, and H. Goronkin, "Submicron Spin Valve Magnetoresistive Random Access Memory Cell" J. Appl. Phys., vol. 81, p. 3992, 1997.

[10] S. Tehrani, E. Chen, M. Durlam, T. Zhu, and H. Goronkin, "High Density Nonvolatile Magnetoresistive RAM," IEDM Technical Digest, vol. 193, 1996.

[11] S. Tehrani, E. Chen, M. Durlam, M. DeHerrera, J.M. Slaughter, J. Shi, and G. Kerszykowski, "High density submicron magnetoresistive random access memory" J. Appl. Phys., vol. 85, p. 5822-27, 1999.

[12] R.D. McMichael, W.F.Egelhoff, Jr., Ha Minh, "Improved thermal stability of GMR spin valve films," Proc. Mag. Ultrathin Films, Multilayers and Surf. Pittsburgh: MRS, 1995, pp. 397-402.

[13] C. Cowache, B. Dieny, S. Auffret, M. Cartier, R.H. Taylor, R. O'Barr, S.Y. Yamamoto, "Spin-valve structures with NiO pinning layers", IEEE Trans. Mag., vol. 34, pp. 843-5, 1998.

[14] R.C. Sousa, J. J. Sun, V. Soares, P.P. Freitas, A. Kling, M.F.da Silva, J.C. Soares, "Large tunneling magnetoresistance enhancement by thermal annel", Appl. Phys. Lett., vol. 73, pp. 3288-90, 1998.

[15] M. Sato, H. Kikucho, K. Kobayashi, "Ferromagnetic tunnel junctions with plasma-oxidized Al barriers and their annealing effects" J. Appl. Phys., vol. 83, pp. 6691-3, 1998.

[16] J. Shi, T. Zhu, M. Durlam, E. Chen, S. Tehrani, Y.F. Zheng, and J.-G. Zhu, "End Domain States and Magnetization Reversal in Submicron Magnetic Structures" IEEE Trans. Magn., vol. 34, p. 997, 1998.

[17] J. Shi, S. Tehrani, T. Zhu, Y.F. Zheng and J. G. Zhu, "Magnetization vortices and anomalous switching in patterned NiFeCo submicron arrays," Appl. Phy. Lett., vol.74, p.2525-7, 1999.

[18] R.E. Scheuerlein, "Magneto-Resistive IC Memory Limitations and Architecture Implications," Proc. 7th IEEE Intl. Nonvolatile Memory Technology Conference. New York: IEEE, 1998, pp. 47-50.

[19] S. Lai, "Tunnel Oxide and ETOXtm Flash Scaling Limitation Proc. 7th IEEE Intl. Nonvolatile Memory Technology Conference. New York: IEEE, 1998, p.6-7.